

REMARKS

Claims 40, 43-51, 68-72, and 74-86 remain pending. Applicant respectfully requests reconsideration of the above-referenced application in light of the foregoing remarks.

At the outset, Applicant acknowledges with appreciation that claims 76-86 are in condition for allowance. Applicant respectfully submits that claims 40, 43-47, 68, 71-72, and 74-75, also contain allowable subject matter. Specifically, the cited references, alone or in combination, do not disclose or suggest "at least one solder contact ball formed *in the second insulator layer*," as recited in claim 40 (emphasis added). Yamamoto's solder bump 48 is formed *only* in Yamamoto's *third* insulating layer 47. Moreover, even *if* Yamamoto's insulating layer 47 is analogous to Applicant's claimed second insulating layer as the Office Action asserts (pg. 2), Yamamoto does not disclose or suggest, "at least one solder contact ball formed *in the first insulating layer*," as recited in claim 71 (emphasis added). A more detailed explanation in response to the rejections is presented below.

Claims 40, 43-49, 68, 71-72 and 74-75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No.: 5,925,931 ("Yamamoto") in view of U.S. Patent No.: 6,249,347 ("Svetkoff"). The rejection is respectfully traversed.

Claim 40 recites a semiconductor device comprising, *inter alia*, "at least one metal layer . . . a first insulator layer formed on said at least one metal contact layer; at least one metal pad . . . a second insulator layer formed on said at least one metal pad . . . and at least one solder contact ball formed *in the second insulator layer* . . . having a diameter less than 100 microns." (emphasis added).

Claim 71 recites a semiconductor device with at least one metal contact layer comprising, *inter alia*, "a first insulating layer formed over and in contact with said at least one metal contact layer; and at least one solder contact ball formed *in the first insulating layer* . . . [which] has a diameter between 2 and 100 microns." (emphasis added).

The Office Action asserts that element 41 is a first insulator layer and element 47 is Yamamoto's second insulator layer (Office Action, pg. 2). Applicant respectfully disagrees. There are at least *three* insulating layers in Yamamoto's FIG. 7. Yamamoto discloses "a protective layer 24 of silicon oxide or silicon nitride." (Col. 4, ll. 26-27). Then, "an insulating layer 41 of an epoxy resin . . . is formed . . . on the *whole upper surface* of the protective layer 24." (Col. 4, ll. 35-38). Finally, protective layer 47 is formed *on* insulating layer 41 (FIG. 7). As a result, Yamamoto discloses a first insulating layer 24, a second insulating layer 41, and a *third* insulating layer 47. In FIG. 7, solder bump 48 is formed *only* in Yamamoto's *third* insulating layer 47.

As a result, solder bump 48 is *not* formed in a *second* insulating layer 41; but, is formed in a *third* insulating layer 47, much less being formed in a *first* insulating layer 24. Yamamoto does not disclose or suggest "at least one solder contact ball formed *in the second insulator layer*," as claim 40 recites (emphasis added), or "at least one solder contact ball formed *in the first insulating layer*," as claim 71 recites (emphasis added).

Moreover, even assuming *arguendo*, that Yamamoto's element 41 corresponds to Applicant's claimed first insulator layer as the Office Action asserts, the second insulating layer in FIG. 7 would be element 47. Consequently, Yamamoto's solder bump would *not* be formed in a first insulating layer as claim 71 recites.

The Office Action acknowledges that Yamamoto does not teach or suggest a solder ball contact that is less than 100 microns in diameter or one that is 2 to 100 microns in diameter (Office Action, pg. 3). Svetkoff is relied upon for disclosing a ball grid array device using solder balls that are 10 to 300 microns in diameter. Svetkoff, however, adds nothing to rectify the deficiencies associated with Yamamoto.

Claims 43-49, 68, and 74-75 depend from claim 40. Claim 72 depends from claim 71. Claims 43-49, 68, 72, and 74-75 should be similarly allowable along with their base claims for at least the reasons provided above, and on their own merits.

For example, as discussed above, Svetkoff is relied upon for disclosing a ball grid array device using solder balls that are 10 to 300 microns in diameter (Office Action, pg. 3). The cited references, even in combination, would still fail to disclose or suggest "solder contacts [that] have a diameter *less* than 10 microns," as recited in claim 43 (emphasis added), or "solder contacts [that] have a diameter of *approximately* 2 microns," as recited in claim 44 (emphasis added), or that "at least one solder contact has a *diameter of approximately* 2 microns," as recited in claim 71 (emphasis added). Svetkoff and Yamamoto would *only* teach a solder ball that is 10 microns or greater in diameter. These are additional reasons for the allowance of dependent claims 43, 44, 68, and 71.

Claims 50 and 51 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto and Svetkoff, and further in view of the admitted prior art. The rejection is respectfully traversed.

Claims 50 and 51 depend from claim 40 and should be allowable for at least the reasons provided above regarding claim 40, and on their own merits. Specifically, Yamamoto and Svetkoff do not disclose or suggest at least one solder contact ball

formed *in the second insulator layer*. Yamamoto discloses three insulating layers, 24, 41, and 47. Yamamoto's solder bump 48 is formed in the *third* insulating layer 47 and *not* the *second* insulating layer 41. The admitted prior art is relied upon for disclosing a semiconductor device bonded to a module substrate or a circuit board, and adds nothing to rectify the deficiencies associated with Yamamoto and Svetkoff.

Claim 69 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto and Svetkoff, and further in view of U.S. Patent No.: 5,888,884 ("Wojnarowski"). The rejection is respectfully traversed.

Claim 69 depends from claim 40 and should be similarly allowable for at least the reasons provided above regarding claim 40, and on its own merits. In particular, Yamamoto and Svetkoff do not disclose or suggest at least one solder contact ball formed *in the second insulator layer*. Yamamoto discloses three insulating layers, 24, 41, and 47. Yamamoto's solder bump 48 is formed in the *third* insulating layer 47 and *not* the second insulating layer 41. Wojnarowski is relied upon for disclosing a pad metallization comprising four or more layers, and adds nothing to rectify the deficiencies of Yamamoto and Svetkoff.

Claim 70 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto, Svetkoff and Wojnarowski, and further in view of JP Pat. 408236938 ("Takashi"). The rejection is respectfully traversed.

Claim 70 depends from claim 69 which depends from claim 40. Claim 70 should be allowable for at least the reasons provided above regarding claims 40 and 69, and on its own merits. For example, Yamamoto and Svetkoff do not disclose or suggest at least one solder contact ball formed *in the second insulator layer*. Yamamoto discloses three insulating layers, 24, 41, and 47. Yamamoto's solder bump 48 is formed in the

third insulating layer 47 and *not* the *second* insulating layer 41. Takashi is relied upon for disclosing a metal pad comprising Zirconium, and adds nothing to rectify the deficiencies of Yamamoto, Svetkoff, and Wojnarowski.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

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Respectfully submitted,

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